AND8380/D

WDFN6 2x2 μCool™ 506AP Single MOSFET Package Board Level Application Notes and Thermal Performance

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APPLICATION NOTE

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ON Semiconductor

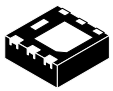
Introduction

New ON Semiconductor μCool™ MOSFETs in a WDFN6 2x2 506AP package are thermally enhanced and remarkably small to exclusively address power management challenges in portable devices such as synchronous buck and boost circuits, high and low side load switches, and lithium−ion battery charging circuits.

This technical note discusses the single−channel WDFN6 506AP package overview, pad patterns, evaluation board layout and thermal performance.

Package Overview

Figure 1 illustrates a single site WDFN6 semiconductor device package and pin−out description. A half etch lead−frame complements mold lock features allowing this leadless package to provide an exposed drain pad for excellent thermal conduction and reduced electrical parasitics. The low profile (< 0.8 mm) compact design is similar to the popular DFN/QFN package allowing for an easy fit in thin environments. Suggested guidelines for mounting criteria on a printed circuit board (PCB) are outlined in application note AND8211/D.



STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

Figure 1. The Underside of a Single−Chip 6 Pin WDFN Package

Basic Pad Pattnes

A recommended solder−mask defined mounting footprint is defined in Figure 2. The WDFN6 506AP footprint dimensions are the same as a standard SC−88 and SC−70−6 package. However, the underside of the 506AP package offers the added feature of an exposed flag acting as a drain contact and heat dissipation path to promote operation at a lower junction temperature.

Figure 3 depicts a minimum recommended pad pattern that confines an improved thermal area of drain connections (Pins 1, 2, 5, 6) to the basic footprint. In addition, increasing the contact area of the exposed source to include Pin 4 promotes a decrease of inductance. A drain copper area of 2.39 sq. mm assists in directing the power dissipation path through the copper lead−frame and into the board. The addition of vias to other board layers further enhances device performance. An evaluation board containing the minimum recommended pad pattern and aforementioned vias is shown in Figure 4 of the subsequent section.

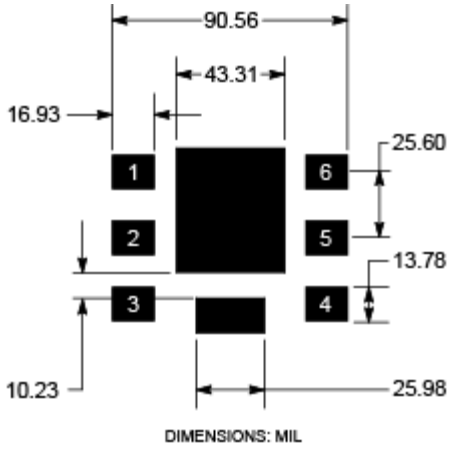


Figure 2. Basic Pad Layout

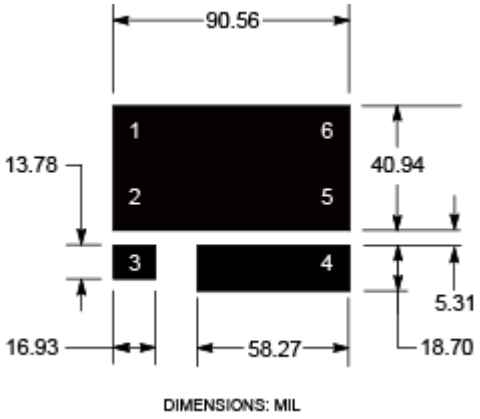
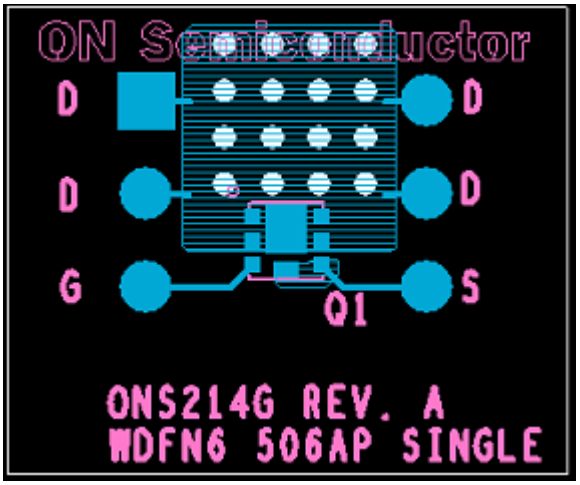


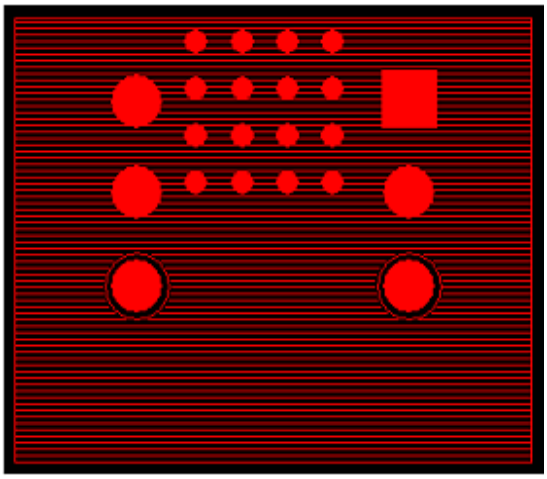
Figure 3. Minimum Recommended Pad Pattern

Evaluation Board

The evaluation board, shown in Figure 4, measures 0.6 x 0.5 inch. The board contains 1 oz. copper thickness on top−side and 1 oz. copper thickness on the underside. Vias are added through to the underside of the board where contact is made with a copper pad area of approximately board size dimensions. On top−side, the copper pad area surrounding the four drain leads is increased to approximately 0.0544 square inch resulting in a total dissipation path area of 0.3544 square inch.



Front of Board



Back of Board

Figure 4. Evaluation Board

This 6−pin DIP design allows the use of sockets and facilitates wire interfacing. Figure 5 represents a WDFN6 506AP package mounted on the evaluation board with and without test pins. A quick thermal analysis of this board is conducted by inducing a saturation current of 820 mA. This yields a junction temperature of 79.4°C and a board temperature of 63.6°C. Figure 6 shows a thermal image of this board under the aforementioned conditions.

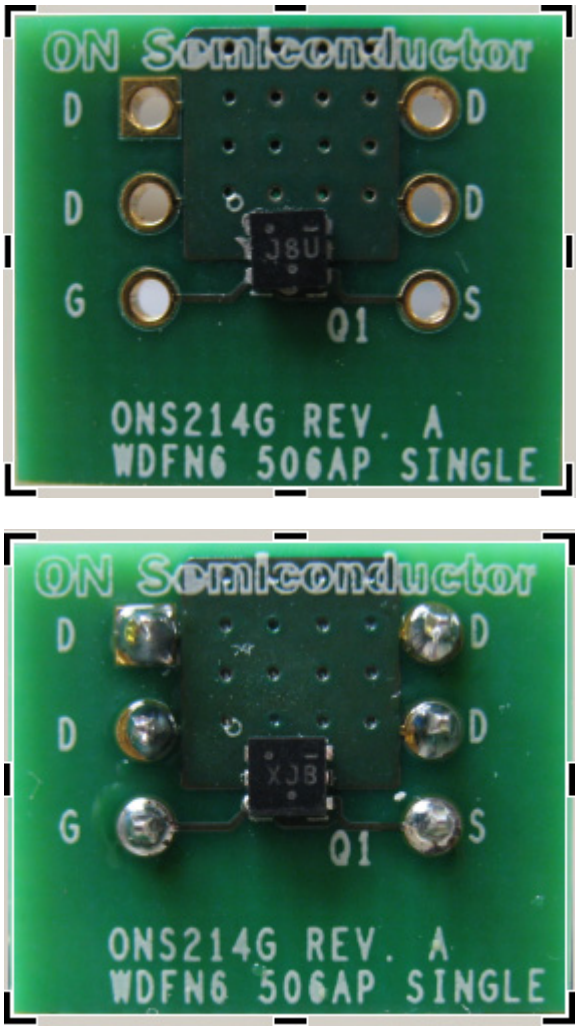


Figure 5. Mounted Device

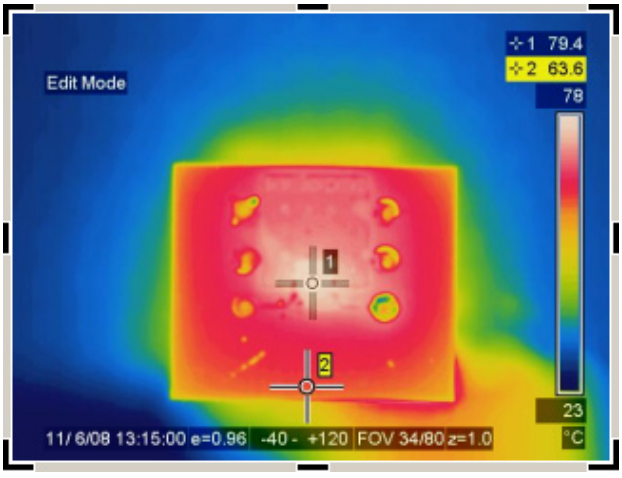


Figure 6. Thermal Image of Mounted Device

Further results from the measured thermal performance of this package are described in the subsequent section. Testing included a thermal analysis of the package surface mounted on a FR4 board using one−inch square pad size and the minimum recommended pad size.

THERMAL PERFORMANCE

Assumptions and Definitions

The subsequent sections outline the thermal performance of a WDFN6 506AP package. All values and equations are obtained from simulations and pertain to the Theta(DC) matrix unless otherwise specified. A 10% duty cycle is arbitrarily chosen to evaluate various thermal responses. Refer to Figure 11 for thermal responses at varying duty cycles. The simulation models used to derive the results in this section are modeled around results obtained from physical testing and are considered reliable. Table 1 defines a set of parameters used throughout this section.

Table 1. THERMAL ANALYSIS PARAMETERS

Symbol	Definition
T_J	Junction Temperature
T_A	Ambient Temperature
P_D	Power Dissipation
$R_{\theta-JL}$	Thermal Resistance from Junction to Location "L"
$R(u)_{EFF}$	Effective (maximum) Thermal Resistance of Package
Ψ_{Fn-L}	Thermal Reference between Foot "n" and location "L"
Ψ_{J-L}	Thermal Reference between Junction and location "L"

The number designation associated with "foot" in the subscript of each Ψ (read psi) term corresponds to the pin identification number as shown in Figure 7.

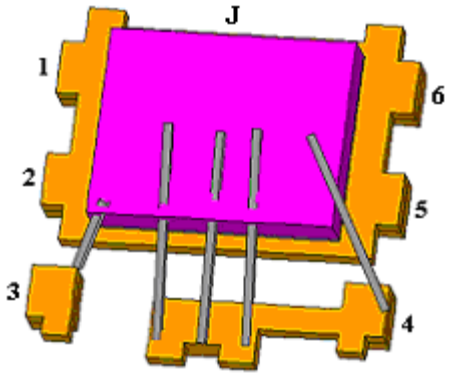


Figure 7. Foot and Junction Identification

Figures 8 and 9 represent Cauer and Foster Ladders respectively. This technical note assumes the reader has a general understanding of these networks. Please refer to the documentation cited under references for detailed descriptions of thermal RC networks. In this section, the Foster network is used to calculate various thermal characteristics. For example, as seen in Figure 9, a particular thermal resistance occurs between the junction and C1/C2 node (denoted here as Ψ_{J-L}). Then, the sum of all thermal resistances between the C1/C2 node and the Cn−1/Cn node is called a junction−to−foot thermal *reference* (Ψ_{J-Fn}). Therefore, in the case of Figure 9, the junction−to−ambient thermal *resistance* ($R_{\theta JA}$) is measured as the sum of thermal references such that,

$$R_{\theta JA} = \Psi_{JFn} + \Psi_{FnA} \qquad \text{(eq. 1)}$$

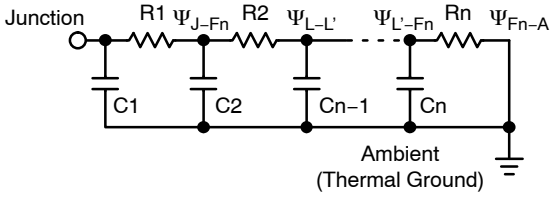


Figure 8. Grounded Capacitor Thermal Network ("Cauer" Ladder)

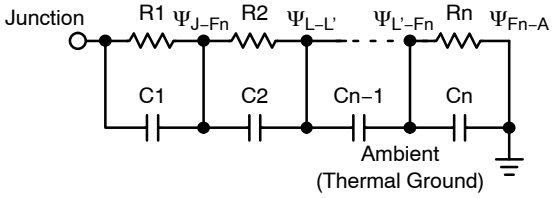


Figure 9. Non−Grounded Capacitor Thermal Network ("Foster" Ladder)

Junction−to−Foot/Foot−to−Ambient

The Foster Network junction−to−foot thermal references and foot−to−ambient thermal references under steady state conditions are outlined in Table 2.

Table 2. THERMAL REFERENCE PARAMETERS

10% Duty Cycle	Junction−to−Foot	
	Min−Pad Size	1 in sq. Pad
P_D	0.7 W	1.9 W
Copper Area	30 mm^2 (2 oz)	1.127 in^2 (2 oz)
Ψ_{JF2}	13.9°C/W	15.2°C/W
Ψ_{JF3}	51.1°C/W	26.3°C/W
10% Duty Cycle	**Foot−to−Ambient**	
	Min−Pad Size	**1 in sq. Pad**
P_D	0.7 W	1.9 W
Copper Area	30 mm^2 (2 oz)	1.127 in^2 (2 oz)
Ψ_{F2A}	172.4°C/W	54.5°C/W
Ψ_{F3A}	135.2°C/W	43.4°C/W

A relationship for the thermal resistance ($R_{\theta-JnA}$) of each device is established by using either of the following relationships,

$$R_{\theta JA} = \Psi_{JF2} + \Psi_{F2A} \qquad \text{(eq. 2)}$$

$$R_{\theta JA} = \Psi_{JF3} + \Psi_{F3A} \quad \text{(eq. 3)}$$

Substituting appropriate values, from Table 2, into the above equations yields $R_{\theta JA}$ = 69.7°C/W for the one−inch square pad size and $R_{\theta JA}$ = 186.3°C/W for min pad size.

Junction−to−Ambient

Table 3 outlines the junction−to−ambient thermal analysis of the WDFN6 506AP package surface mounted on an FR4 board. Substituting values from Table 3 into Equation 4 allows various junction temperatures to be calculated at assumed ambient temperatures.

$$T_J = R_{\theta JA} \times P_D + T_A \quad \text{(eq. 4)}$$

The effective thermal resistance of the package, $R(u)_{EFF}$, is defined as a function of DC or transient response. These two cases are modeled by Equations 5 and 6 respectively.

$$R(DC)_{EFF} = \frac{\left(T_J - T_A\right)}{P_D} \quad \text{(eq. 5)}$$

$$R(t)_{EFF} = \frac{\left(T_{J(Pulse)} - T_A\right)}{P_D} \quad \text{(eq. 6)}$$

Table 3. JUNCTION−TO−AMBIENT THERMAL CHARACTERISTICS

	Steady State		Pulsed Time = 5 seconds
10% Duty Cycle	**1 in sq. Pad**	**Min−Pad Size**	**1 in sq. Pad**
Copper area	1.127 in^2 [2 oz]	30 mm^2 [2 oz]	1.127 in^2 (2 oz)
T_A	25.0°C	25.0°C	25.0°C
P_D	1.90 W	0.70 W	1.90 W
$R_{\theta JA}$	69.7°C/W	186.3°C/W	69.7°C/W*
$R_{(DC)EFF}$			
$R(singlepulse)_{EFF}$			38.2°C/W*
$R(pulsed)_{EFF}$			41.3°C/W
T_J	157.4°C	155.4°C	157.4°C
T_J (single pulse)			97.5°C*
T_J (pulsed)			103.5°C*

*Refer to Appendix−A for R(t) Derivation

Junction−to−Board

Table 4 outlines the junction−to−board thermal analysis of the WDFN6 506AP package surface mounted on an FR4 board. Substituting values from Tables 2 and 4 into Equation 7 allows various junction temperatures to be calculated at assumed board temperatures.

$$T_J = P_D \times \left(R_{\theta JA} - \Psi_{F2A}\right) + T_{BOARD} \qquad \text{(eq. 7)}$$

Table 4. JUNCTION−TO−BOARD THERMAL CHARACTERISTICS

10% Duty Cycle	Steady State		Pulsed time = 5 seconds
	1 in sq. Pad	Min−Pad Size	1 in sq. Pad
Cu area	1.127 in^2 [2 oz]	30 mm^2 [2 oz]	1.127 in^2 [2 oz]
P_D	1.90 W	0.70 W	1.90 W
T_A	25.0°C	25.0°C	25.0°C
T_{BOARD} (DC)	128.5°C	145.7°C	128.5°C
T_{BOARD}(single)			
T_{BOARD}(pulsed)			
$T_{J\ (DC)}$	157.4°C	155.4°C	157.4°C
T_J (single pulse)			97.5°C
T_J (pulsed)			103.5°C
$R_{\theta-A}$ (DC)	69.7°C/W	186.3°C/W	69.7°C/W
$R_{\theta JA}$ (single pulse)			38.2°C/W
$R_{\theta JA}$ (pulsed)			41.3°C/W

*Refer to Appendix−A for R(t) Derivation

SUMMARY

Figure 10 illustrates a steady state plot of the change in thermal resistance and max power dissipation that occurs with a change in the amount of copper spread across a given area. Evaluating the plots at the minimum recommended pad size and one−inch square pad size yields the following maximum values:

Table 5. MAXIMUM RATINGS FROM FIGURE 10

10% Duty Cycle	Min−Pad Size		1 in sq. Pad	
Cu area (Cu thk)	30 mm^2 (1 oz)	30 mm^2 (2 oz)	1.127 in^2 (1 oz)	1.127 in^2 (2 oz)
$R_{\theta J1A}$	222.4°C/W	186.3°C/W	82.7°C/W	69.7°C/W
Max Power	0.562 W	0.671 W	1.51 W	1.794 W

Figure 11 illustrates the packages change in effective thermal resistance with respect to pulse time. The plot reflects data sampled at a minimum recommended pad size (2 oz. Cu). Under steady state conditions the plot yields $R(t)_{EFF}$ = 186.34°C/W. Maintaining steady state conditions and increasing the copper area to 1.0 square inch, 2 oz Cu, will yield $R(t)_{EFF}$ = 69.68°C/W. These results show that this package exhibits more efficient thermal characteristics than the aforementioned SC−88 package. Although a SC−88 package carries the same footprint dimensions as a WDFN6 506AP, the minimum recommended pad size plot evaluated under steady state conditions yields $R(t)_{EFF}$ = 352.4°C/W. The decreased thermal resistance of a WDFN6 506AP package is attributed to the exposed flag acting as a drain contact and heat dissipation path.

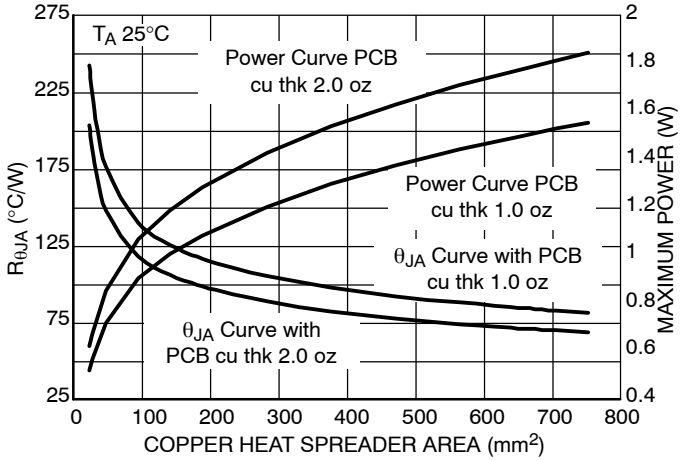


Figure 10. Self−Heating Thermal Characteristics as a Function of Copper Area on the PCB

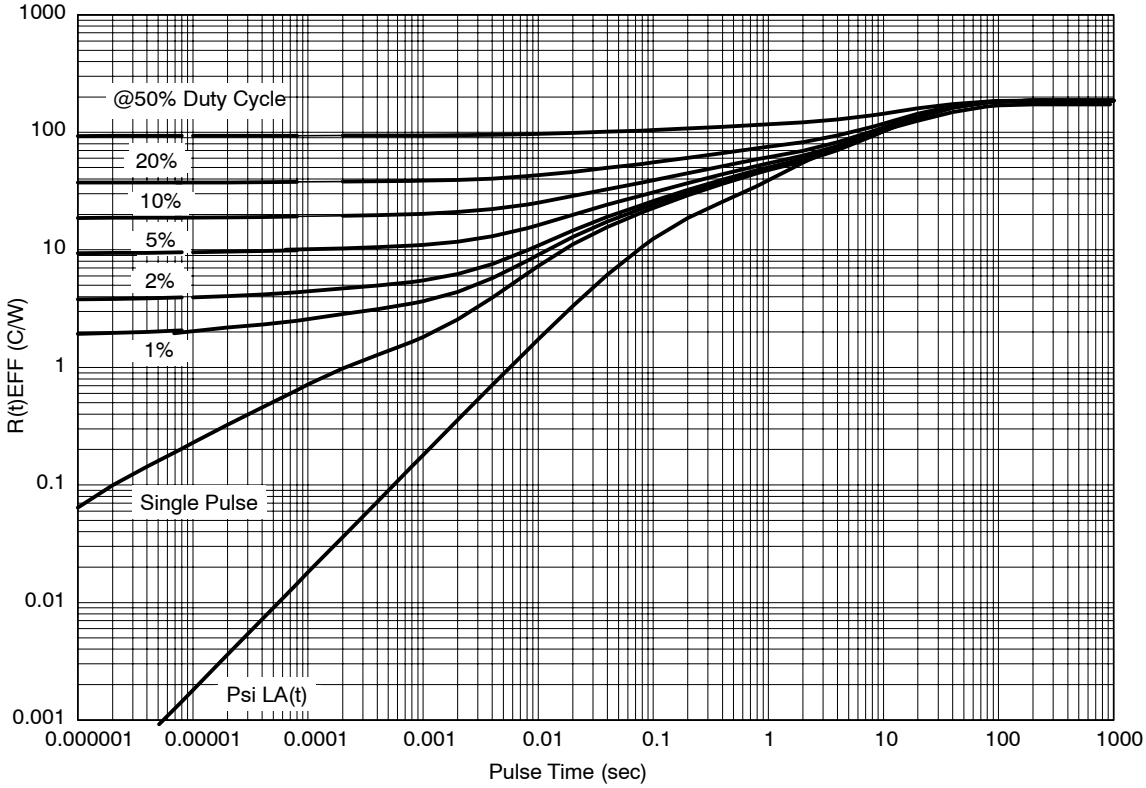


Figure 11. Thermal Response Minimum Pad Size

References

1. R.P. Stout, D.T. Billings, “How to Extend a Thermal−RC−Network Model (Derived From Experimental Data) to Respond to an Arbitrarily Fast Input,” *ON Semiconductor*, 2006.
2. R.P. Stout, “Thermal RC Ladder Networks; Packaging Technology Development ,” *ON Semiconductor*, 2006.
3. R.P. Stout, “General Thermal Transient RC Networks,” *ON Semiconductor*, 2006.

APPENDIX

Junction−to−Ambient Theta(t) Derivation

Equation 8 describes the relationship used to derive a model describing temperature rise for a single pulse application (see Table 6).

$$R(t)_{\theta JA} = \sum_{n=1}^{m} \Psi_n \times \left[1 - \exp(-t/\tau_n)\right] \quad \text{(eq. 8)}$$

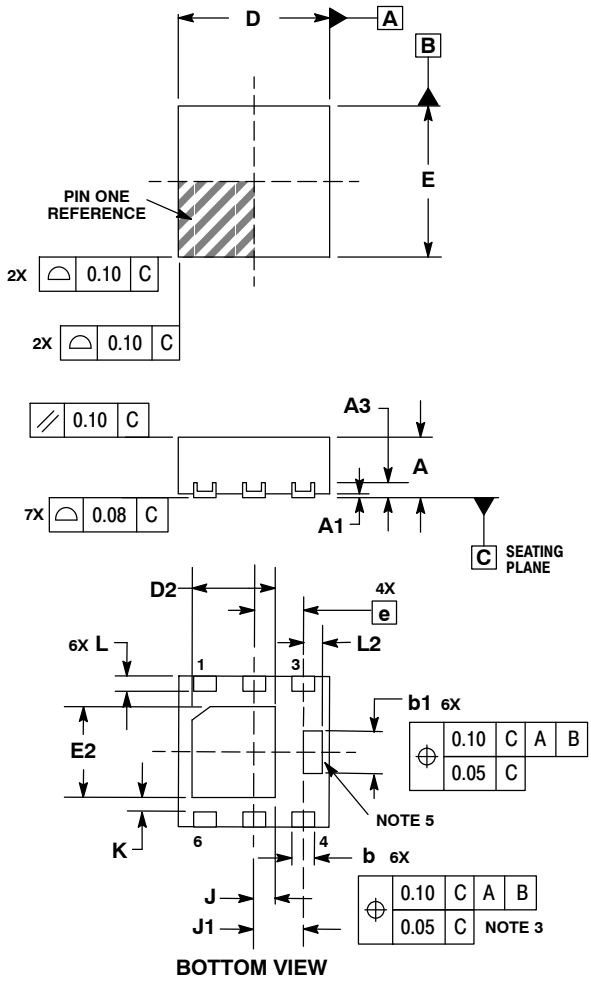
Where $R(t)_{\theta JA}$ is the total resistance of the network, Ψ_n is the resistance node, t is the length of a single pulse in seconds and τ_n (tau) is the characteristic time of ladder. Assuming square wave impulses, the peak junction temperature is estimated by substituting $R(t)_{\theta JA}$ into Equation 4.

Table 6. FOSTER NETWORK

	1” Pad (2 oz. Cu)		Min Pad (2 oz. Cu)	
n	R (C/W)	Tau (sec)	R (C/W)	Tau (sec)
1	0.068	1.0E−06	0.068	1.0E−06
2	0.148	1.0E−05	0.148	1.0E−05
3	0.466	1.0E−04	0.466	1.0E−04
4	0.347	2.3E−04	0.347	2.3E−04
5	8.42	0.0140	8.42	0.0140
6	9.92	0.071	9.92	0.071
7	6.4	0.340	6.4	0.340
8	4.0	4.41	15.4	0.42
9	7.9	1.67	64.3	10.98
10	32	72.4	80.9	31.3

PACKAGE DIMENSIONS

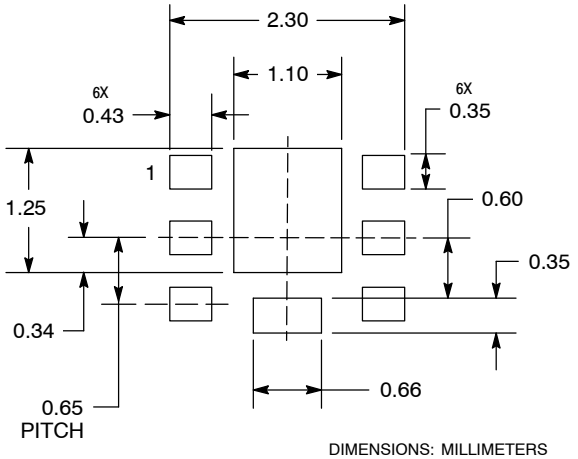
WDFN6 2x2
CASE 506AP−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. CENTER TERMINAL LEAD IS OPTIONAL. TERMINAL LEAD IS CONNECTED TO TERMINAL LEAD # 4.
6. PINS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
b1	0.51	0.61
D	2.00 BSC	
D2	1.00	1.20
E	2.00 BSC	
E2	1.10	1.30
e	0.65 BSC	
K	0.15 REF	
L	0.20	0.30
L2	0.20	0.30
J	0.27 REF	
J1	0.65 REF	

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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